U.S. EXPRESS MAIL LABEL NO.: EL 752587395 US IC17 Rec'd PCT/PTO 0 1 JUN 2001

FORM PTO-1390 (Modified) (REV 5-93) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTORNEY'S DOCKET NUMBER
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		078986/0203
		U S. APPLICATION NO. (If known, see 37 C.F.R. 1.5) 09/857503
INTERNATIONAL APPLICATION NO. **PCT/GB99/03897**	INTERNATIONAL FILING DATE **24 November 1999**	PRIORITY DATE CLAIMED **4 December 1998**

TITLE OF INVENTION
A SERIAL-PARALLEL BINARY MULTIPLIER

APPLICANT(S) FOR DO/EO/US
ANDREW DEWHURST

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   - ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   - ☒ has been transmitted by the International Bureau.
   - ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   - ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   - ☐ have been transmitted by the International Bureau.
   - ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   - ☐ have been made and filed in the United States Receiving Office.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☐ Other items or information: Copy of International Search Report (2 pages)

U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.50)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
Unknown 09/857503	PCT/GB99/03897	078986/0203

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee (37 CFR 1.492(a)(1)-(5): Search Report has been prepared by the EPO or JPO.....$0.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482).....$710.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2) $0.00		
Neither international preliminary examination fee (37 CFR 1.482) nor International search fee (37 CFR 1.445(a)(2)) paid to USPTO $0.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $0.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$710.00	
Surcharge of $130.00 for furnishing the oath or declaration later than 20 Months from the earliest claimed priority date (37 CFR 1.492(e))		

Claims	Number Filed		Included in Basic Fee		Extra Claims		Rate		
Total Claims	11	-		=		×	$18.00		
Independent Claims	2	-		=		×	$78.00		
Multiple dependent claim(s) (if applicable)								$0.00	
TOTAL OF ABOVE CALCULATIONS =									
Reduction by ½ for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).									
SUBTOTAL =									
Processing fee of $130.00 for furnishing English translation later the 20 months from the earliest claimed priority date (37 CFR 1.492(f). +									
TOTAL NATIONAL FEE =								$0.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +									
TOTAL FEES ENCLOSED =								$710.00	

				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of $790.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. **50-0872** in the amount of **$** to the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-0872. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Foley & Lardner
2029 Century Park East, Suite 3500
Los Angeles, California 90067-3021
Telephone: (310) 975-7963

SIGNATURE

NAME TED R. RITTMASTER

REGISTRATION NUMBER 32,933

U.S. Express Mail Label No.: EL 752587395 US

09/857503
JC18 Rec'd PCT/PTO 0 1 JUN 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application:	Andrew Dewhurst	Examiner:	Unassigned
Serial No.	Unassigned	Group Art Unit:	Unassigned
Filing Date:	Herewith	Attorney Docket No.	078986/0203
Title:	A SERIAL-PARALLEL BINARY MULTIPLIER		

CERTIFICATE UNDER 37 CFR 1.8: I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on June 1, 2001.

Richard S. Ruggiero

Richard S. Ruggiero

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, DC 20231

Dear Sir:

Prior to the first Office Action, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the specification, at page 2, after line 9, to add the following paragraphs:

US-A-5539685 describes the conventional process of multiplication by repeated shift and add operations. An improved high-speed multiplier device is then described. The improved devices requires both the operands to be loaded into separate register before the shift and addition process is commenced. The latter process is first completed before the partial process product is stored in a temporary register. Since each process is dependent on the previous process being complete, the multiplication operation is still relatively time consuming.

In Computer Design (Pennwell Publ. - US ISSN 00104566) Volume No. 5, May 1972,Pages 115-121, XP-002130443 an article entitled "2's Complement Arithmetic Operations" by S. Sklar describes the technique of Booth Coding for 2's complement multiplication. This technique provides a multiplication process with performance improvements. An arithmetic operation is performed on one operand by reference to decoded bits of a second operand. The required arithmetic operation is determined by the results of the decoding process.

JP03116327 describes a high speed multiplier. Multiples of a first operand are pre-calculated and made available at a selector. The selection of the appropriate operand multiple is made according to the current pair of bits of the second operand. The selection requires the presence of both current bits of the second operand and only then can the addition operation be performed.

IN THE CLAIMS:

Please replace original 1-11 with new claims 12-18 as follows:

12. (new) A serial binary multiplier for multiplying two binary operands in two's complement form to provide a final product, the multiplier comprising means for storing at least one first operand, a register for storing a partial product of the multiplication operation, means for receiving bits of a second operand serially, a calculation unit comprising an adder and a subtractor for selectively adding or subtracting the element of the first operand to or from the partial product means for selecting either the result output from the calculation unit or the currently stored partial product on the basis of the second operand and entering it into the partial product register, means for shifting the partial product in the register to provide a new partial product, and means to output the contents of the register as the final product when all bits of the second operand have been received.

13. (new) A serial binary multiplier according to claim 1 , wherein the calculation unit is a single circuit capable of addition and subtraction operations, the operation being determined by the value of the previously received bit of the second operand.

14. (new) A serial binary multiplier according to claim 1, the add or subtract operation of the calculation unit is performed simultaneously with transmission of the current data bit of the second operand.

15. (new) A serial binary multiplier according to claim 1, wherein the mean for selecting is a decoder.

16. (new) A method of operating a serial binary multiplier for multiplying two binary operands in two's compliment form to provide a final product compromising the steps of storing a first operand, storing a partial product in a register, transmitting

bits of a second operand serially whilst simultaneously adding or subtracting the first operand to or from the partial product, selecting either the result from the addition or subtraction or the currently stored partial product on the basis of the value of the received bit of the second operand and entering it into the partial product register, shifting the partial product in the register to provide a new partial product, and outputting the contents of the register as the final product when all bits of the second operand have been received.

17. (new) A method according to claim 5, wherein the adding or subtracting operation is selected in response to the value of the previously received bit of the second operand.

18. (new) A method according to claim 5, wherein the adding or subtracting operation is performed simultaneously with transmission of the current data bit of the second operand.

Remarks:

Prior to the first Office Action, please enter the above amendments to the application and claims.

Respectfully submitted,

Dated: June 1, 2001

Ted R. Rittmaster
Reg. No. 32,933

FOLEY & LARDNER
2029 Century Park East
Suite 3500
Los Angeles, CA 90067-3021
Tel: (310) 277-2223
Fax: (310) 557-8475

A SERIAL BINARY MULTIPLIER

The present invention relates to a serial binary multiplier for performing fixed point multiplication in data processing apparatus.

Central processing units of data processing apparatus generally incorporate a multiplier unit for performing multiplication operations. Typically such multiplier units are based on well known array multiplier designs or a shift-and-add algorithm. Multiplier units of this kind are generally optimised for performance (i.e. processing power and speed) or for compact implementation.

One example of a multiplier unit having compact size is described in our co-pending international patent application No. GB97/01520.

However, the performance of a serial multiplier, unlike an array multiplier design, is dependent on the total transmission delay in performing a sequence of operations as the serial data is received. The total transmission delay is a combination of several delays in the sequential operation of the multiplication process, namely: a delay as the data is routed to the input of the multiplier; a delay as the data passes through the interconnect; and the multiplier operation delay.

In monolithic design circuit performance has improved many fold as semiconductor processing techniques have lead to smaller and smaller component geometries. Contemporary integrated circuit process technology enables the manufacture of deep sub-micron circuit elements with physical dimensions of less than one micron. The performance of these circuits is often no longer determined by the operation of the active circuit components but is dominated by the interconnect delay between them.

The difference between the performance of active components, for example transistors, and the interconnect, or routing, is greatly exaggerated in the implementation of programmable circuits such as Field Programmable Gate Arrays (FPGAs), where greater flexibility in the interconnect structures adds further to the delay imposed on signals passing through them.

An alternative known approach to constructing a high performance multiplier is to base the design around a look-up-table. This is demonstrated in Altera's FLEX

10K device. Using this technique all the possible results of the multiplication process are stored in a table and the input operands are used to choose one result from the table. The size of such multipliers becomes very large when, say, operands of 8 bits or more are used. The multiplication of n-bit wide operands requires a table with 2^{2n} entries. An improvement to this design is to use multiple smaller look-up tables followed by a calculation step. This technique is also shown in Altera's FLEX 10K device. The latter technique reduces the size of the multiplier but degrades the performance since a further calculation step is required after a preliminary result has been selected from the look-up table.

US-A-5539685 describes the conventional process of multiplication by repeated shift and add operations. An improved high-speed multiplier device is then described. The improved device requires both the operands to be loaded into separate registers before the shift and addition process is commenced. The latter process is first completed before the partial process product is stored in a temporary register. Since each process is dependent on the previous process being complete, the multiplication operation is still relatively time consuming.

In Computer Design (Pennwell Publ. –US ISSN 00104566) Volume No. 5, May 1972, pages 115-121, XP-002130443 an article entitled "2's Complement Anthimetic Operations" by S.Sklar describes the technique of Booth Coding for 2's complement multiplication. This technique provides a multiplication process with performance improvements. An arithmetic operation is performed on one operand by reference to decoded bits of a second operand. The required arithmetic operation is determined by the results of the decoding process.

JP03116327 describes a high speed multiplier. Multiples of a first operand are pre-calculated and made available at a selector. The selection of the appropriate operand multiple is made according to the current pair of bits of the second operand. The selection requires the presence of both current bits of the second operand and only then can the addition operation be performed.

It is an object of the present invention to obviate or mitigate the aforesaid disadvantages and to improve the performance of the data processing function of multiplication.

According to a first aspect of the present invention there is provided a serial binary multiplier for multiplying two binary operands to provide a final product, the multiplier comprising means for storing at least one first operand, a register for storing a partial product of the multiplication operation, means for receiving elements of a second operand serially, a calculation unit for calculating all possible results being the sum of the partial product and the product of the first operand with all possible values of the element of the second operand, said possible results being calculated during transmission of the second operand, means for selecting either one of the possible results or the currently stored partial product on the basis of the value of the received element of the second operand, means for shifting the partial product in the register to provide a new partial product, and means to output the contents of the register as the final product when all bits of the second operand have been received.

By using the calculation unit to calculate partial products whilst the second operand is transmitted the delay in transmitting the data is less significant in the overall time required to conduct the multiplication process.

Preferably the second operand comprises a plurality of elements each comprising an m-bit word. In an embodiment where m=1 the calculation unit is an adder.

The calculation unit calculates all possible results on the basis of the value of the first operand and the value of previously received elements of the second operand.

The means to output the contents of the register preferably provides the final result in serial form.

In one preferred embodiment the first and second operands and the final product are in two's complement form and the possible results are calculated from the first operand, the partial product and the previously received bit of the second operand. In such an embodiment the calculation unit is an adder and subtractor and may take the form of a single circuit capable of addition and subtraction, the operation being determined by the value of the previously received bit.

According to a second aspect of the present invention there is provided a method of operating a serial binary multiplier for multiplying two binary operands to provide a product comprising the steps of storing a first operand, storing a partial product in a register, transmitting elements of a second operand serially whilst simultaneously calculating all possible results being the sum of the partial product and the product of the first operand with all possible values of the element of the second operand, selecting either one of the possible results or the currently stored partial product on the basis of the value of the received element of the second operand, shifting the partial product in the register to provide a new partial product, and outputting the contents of the register as the final product when all bits of the second operand have been received.

Specific embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a block diagram of an embodiment of an m-bit binary serial multiplier according to a first embodiment of the present invention;

Figure 2 is a block diagram of an embodiment of a 1-bit binary multiplier according to a second embodiment of the present invention;

Figure 3 is a block diagram of the multiplier of figure 2 adapted for two's complement operation according to a third embodiment of the present invention;

Figure 4 is a table showing the calculation process of the multiplier shown in figure 3; and

Figure 5 is a timing diagram for a single cycle of the multiplier operation.

Referring now to the drawings, figure 1 shows the structure of an m-bit serial multiplier which performs the multiplication operation on a locally stored first operand B and a second operand A that is transmitted to multiplier in the form of a serial stream of m-bit wide data elements, the m bits of each data element being received in parallel and multiple serial data elements forming the complete operand data word.

The multiplication process is performed by a calculation unit that comprises a bank of 2^m registers 1 and a bank of 2^m adders 2. The registers 1 store all possible 2^m results of multiplying the first operand B with all possible (2^m) values of the second operand A. Each register 1 within the bank stores one result of multiplying the first operand B with an assumed value of the second operand A. Each of these 2^m multiplication results is passed to one of the adders 2 in the bank of 2^m adders where it is summed with a partial product of the overall multiplication process that is stored in a shift register 3. The results of the addition process are then passed to a multiplexer 4.

A decoder (not shown) receives the m-bit serial input data element of the second operand A and on the basis of this, selects the appropriate correct result via the multiplexer 4. Thus the input data is used to select a pre-calculated result late in the calculation process. The selected (partial) result is then stored in the shift register 3 which reformats the partial result by shifting the stored data by m-bits to the right. The partial result is then recirculated to the input of the bank of adders 2. The multiplication process described above is then repeated for the next received data element of the second operand A until the whole of the input data word of the second operand A has been received and processed. If the input data represents the value zero then the recirculated output of the shift register can simply added to the register 3 rather than selecting the appropriate adder output. The final result in the shift register 3 is transmitted to a parallel to m-bit serial converter (not shown) which outputs the final result (product) in the original m-bit serial format.

The above described multiplier allows the parallel operation of both the multiplier operation (including addition of the products to the partial result in the shift register 3) and the input data transmission. Using a locally stored first operand B a number of possible multiplier results is pre-calculated independently of the second operand A and added to the partial result from the previous cycle. In this way the multiplication process delay and the data transmission delay occur simultaneously, or in parallel. The second operand A is only needed to complete the multiplication process by selecting one of the pre-calculated results. By employing a decoder that selects the appropriate partial result the delay generally associated with the multiplication process is reduced, whilst avoiding the need for a large look-up table of possible results.

It will be appreciated that by using the locally stored first operand B in the preliminary multiplication process, the number of possible pre-calculated results is greatly reduced in comparison to conventional multipliers based on look-up table designs.

Figure 2 shows an embodiment of the present invention that is used to multiply 1-bit serial input data. A 1-bit serial multiplier is highly suited to realisation within a programmable device, since implementing programmable interconnects between functional units that only require a single point-to-point connection is both practical and well known.

The operation of the 1-bit multiplier is similar to that of the generic m-bit multiplier example described earlier, however, using a 1-bit wide input format allows a novel optimisation of the circuit.

Since the input data of the second operand must be either a 1 or a 0 then only one dynamic calculation is required as there are only 2 possible results, one of which is a null operation (i.e. multiplication by zero). The structure of the 1-bit multiplier varies from the m-bit multiplier in that the calculation unit only comprises a single register to store the first operand B and a single adder. Parts corresponding to those of figure 1 are indicated by the same reference numerals increased by 100 and are not further described except insofar as they differ from their counterparts in figure 1.

The calculation unit 1, 2 shown in Figure 1 can be constructed in the 1-bit multiplier embodiment of figure 2 by using a register store for operand B and a single adder 102. The implementation of such a circuit is well known. When the multiplication operation is initiated the previous serial input bit is taken to be a zero. Once the current signal data input bit of the second operand A has been received it is used to determine whether the selected result is to be the result dynamically calculated by the adder (the sum of the received bit of the second operand A and the partial product in the register 103) or the previous partial result (i.e. no operation is performed). The final result is output via a parallel to serial converter 105.

Figure 3 shows a multiplier design for multiplication of 1-bit operands in two's complement format. The serially transmitted second operand A is decoded by a decoder 207 and the output provides instructions to an adder/subtractor 208 to choose the dynamic calculation operation i.e. either to add or to subtract the local operand B to or from the partial result that is fed back from the shift register 203. These add and subtract instructions are decoded from the previous signal data input bit and allow the dynamic calculation to be performed in parallel with the current signal data bit being transmitted. When the multiplication operation is initiated the previous serial input bit is taken to be a zero. Once the current signal data bit has been received and decoded it is used to determine whether the selected result is to be the result dynamically calculated by the multiplier or the previous partial result (i.e. no operation is performed) according to the table shown in figure 4.

The timing diagram for a single cycle of the 1-bit two's complement multiplier operation is shown in Figure 5. The opening part of the clock cycle is available for the independent dynamic calculation of partial result(s) on the basis of the previously received data bit, and for the transmission of the current data bit. This is shown as "Tmult" in Figure 4. The remaining part of the clock cycle is then dedicated to the late select process that requires simple decoding of the current serial input data bit, which may be easily constructed with simple logic gates to give very high performance. The delay attributed to this process is shown as "Tselect" in Figure 4. Clearly, overlapping the data transmission delay and the multiplier operation delay in this late select

multiplier design offers greatly improved performance over traditional serial multipliers.

It will be appreciated that numerous modifications to the above described design may be made without departing from the scope of the invention as defined in the appended claims. For example, the shifting of the partial product stored in the shift register 3, 103, 203 may be performed by any equivalent operation such as modifying the connections to the register. The term "shifting" is used in the claims with the intention of incorporating such equivalent operations.

CLAIMS

1. A serial binary multiplier for multiplying two binary operands to provide a final product, the multiplier comprising means for storing at least one first operand, a register for storing a partial product of the multiplication operation, means for receiving elements of a second operand serially, a calculation unit for calculating all possible results being the sum of the partial product and the product of the first operand with all possible values of the element of the second operand, said possible results being calculated during transmission of the second operand, means for selecting either one of the possible results or the currently stored partial product on the basis of the value of the received element of the second operand, means for shifting the partial product in the register to provide a new partial product, and means to output the contents of the register as the final product when all bits of the second operand have been received.

2. A serial binary multiplier according to claim 1, wherein the elements of the second operand are m-bit words.

3. A serial binary multiplier according to claim 2, wherein m=1 and the calculation unit is an adder.

4. A serial binary multiplier according to claim 1, 2 or 3, wherein the calculation unit calculates all possible results on the basis of the value of the first operand and the value of previously received elements of the second operand.

5. A serial binary multiplier according to any preceding claim, wherein the means to output the contents of the register provides the final result in serial form.

6. A serial binary multiplier according to any preceding claim, wherein the first and second operands and the final product are in two's complement form and the

possible results are calculated from the first operand, the partial product and the previously received bit of the second operand.

7. A serial binary multiplier according to claim 6, wherein the calculation unit is an adder and subtractor.

8. A serial binary multiplier according to claim 7, wherein the calculation unit is a single circuit capable of addition and subtraction, the operation being determined by the value of the previously received bit.

9. A method of operating a serial binary multiplier for multiplying two binary operands to provide a product comprising the steps of storing a first operand, storing a partial product in a register, transmitting elements of a second operand serially whilst simultaneously calculating all possible results being the sum of the partial product and the product of the first operand with all possible values of the element of the second operand, selecting either one of the possible results or the currently stored partial product on the basis of the value of the received element of the second operand, shifting the partial product in the register to provide a new partial product, and outputting the contents of the register as the final product when all bits of the second operand have been received.

10. A serial binary multiplier substantially as hereinbefore described with reference to the accompanying drawings.

11. A method of operating a serial binary multiplier substantially as hereinbefore described with reference to the accompanying drawings.

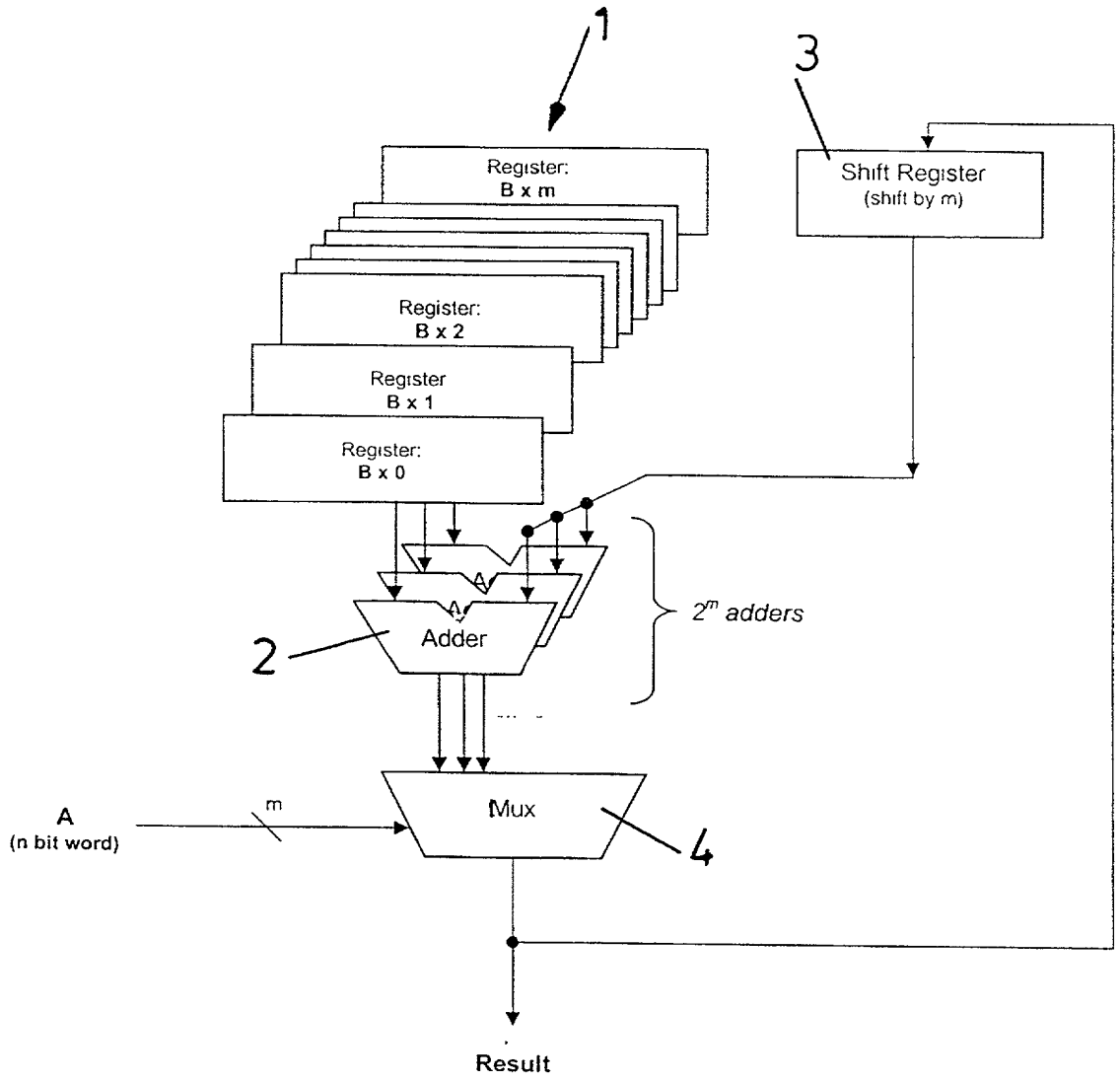
1
3
Register:
B x m
Register:
B x 2
Register
B x 1
Register:
B x 0
Shift Register
(shift by m)
Adder
2
2^m adders
A
(n bit word)
m
Mux
4
Result

FIG. 1

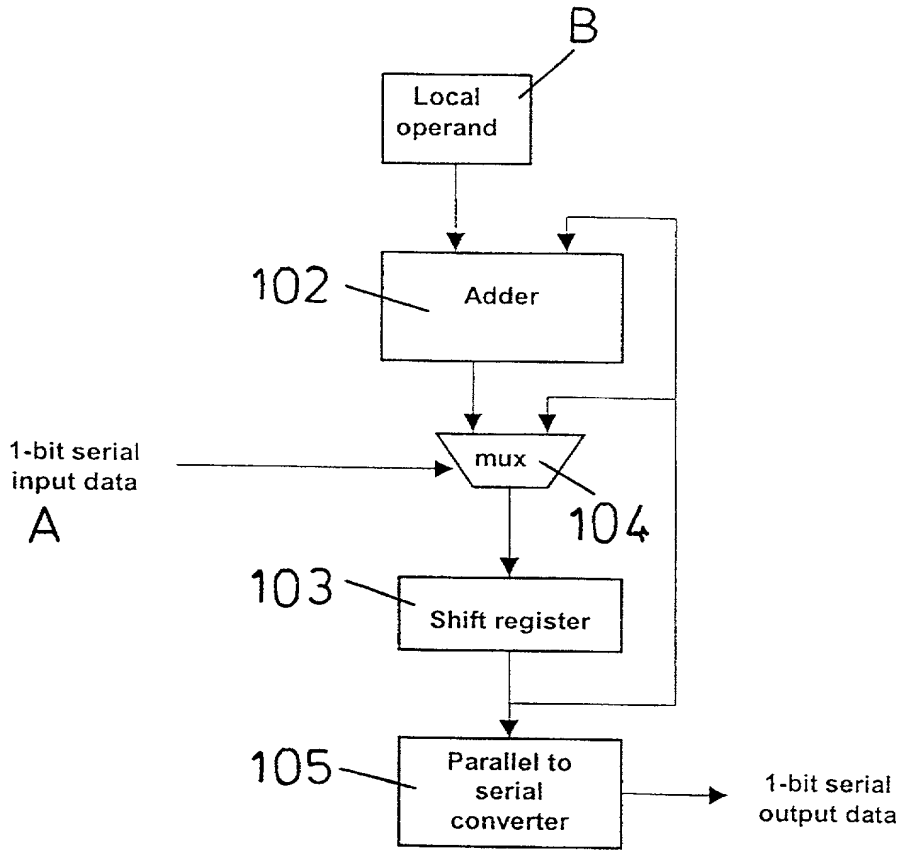
B
Local operand
102
Adder
1-bit serial input data
A
mux
104
103
Shift register
105
Parallel to serial converter
1-bit serial output data

FIG. 2

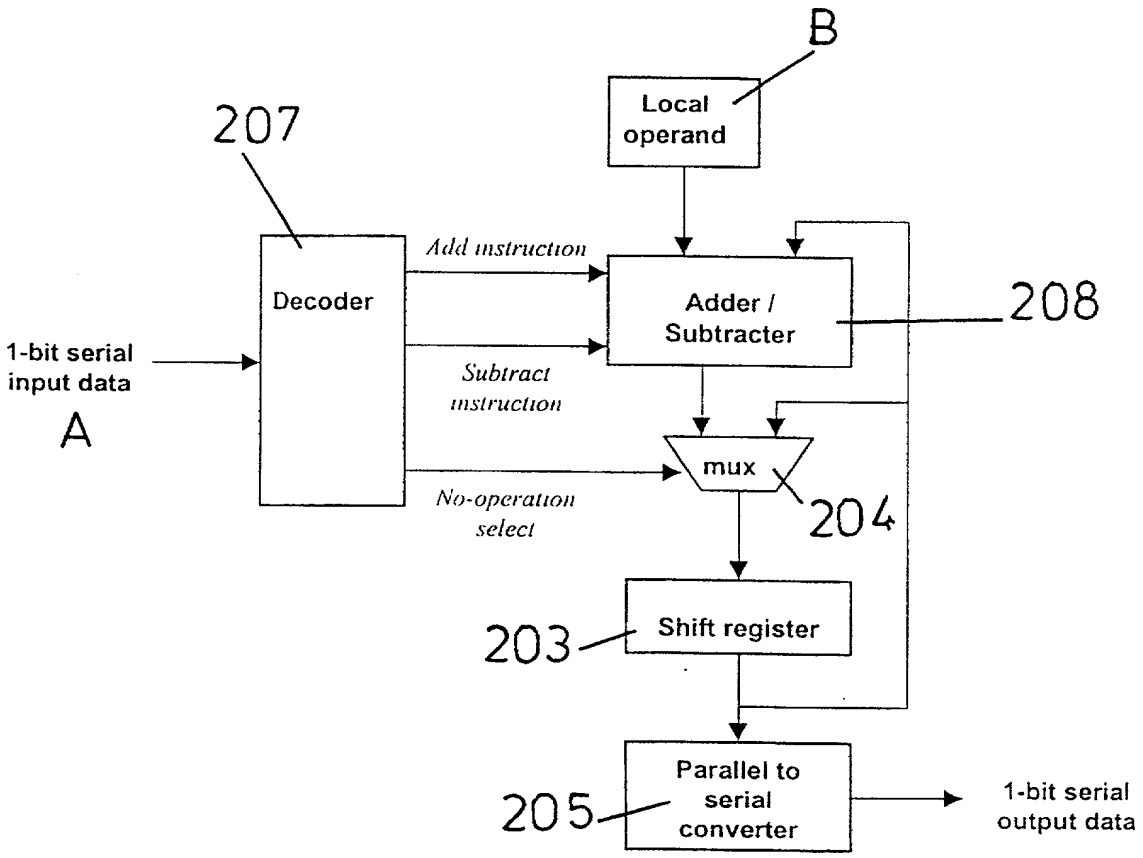
B
Local operand
207
Decoder
Add instruction
Adder / Subtracter
208
1-bit serial input data
A
Subtract instruction
mux
204
No-operation select
203
Shift register
Parallel to serial converter
205
1-bit serial output data

FIG. 3

Current serial input bit	Previous serial input bit (or 0 in first instance)	Pre-calculation	Selected result
0	0	Subtract local operand from partial result	No operation
1	0	Subtract local operand from partial result	Pre-calculated result
1	1	Add local operand to partial result	No operation
0	1	Add local operand to partial result	Pre-calculated result

FIG. 4

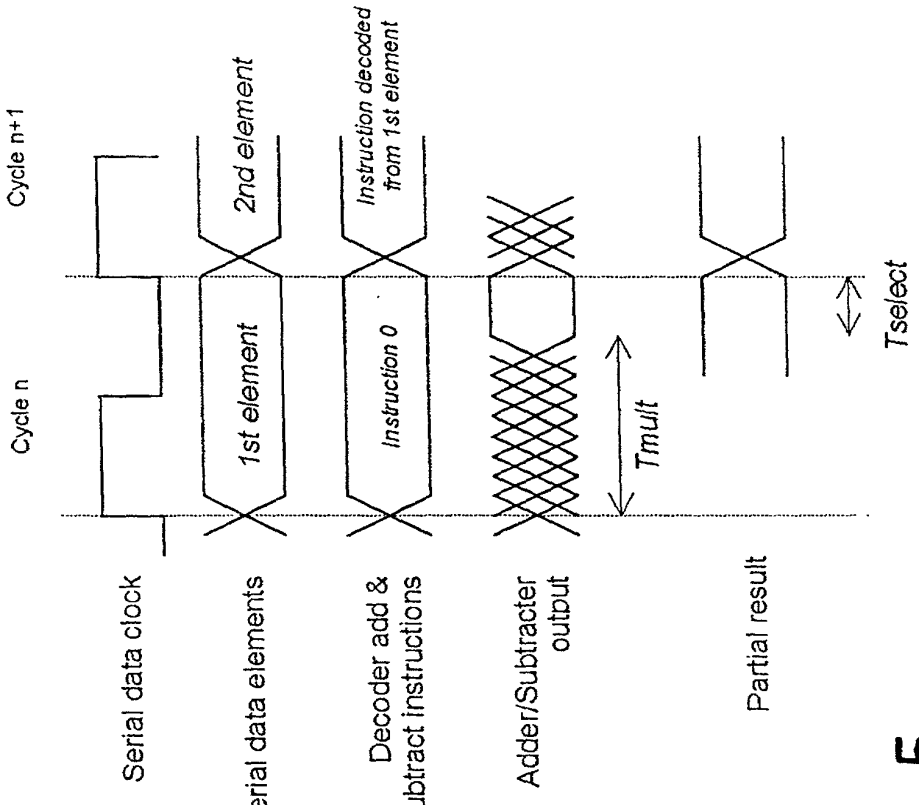
Cycle n
Cycle n+1
Serial data clock
Serial data elements
1st element
2nd element
Decoder add & subtract instructions
Instruction 0
Instruction decoded from 1st element
Adder/Subtracter output
Tmult
Partial result
Tselect

FIG. 5

Docket No. 078986-0203

DECLARATION AND POWER OF ATTORNEY

As below named inventors, we hereby declare: THAT my residence, post office address and citizenship is as stated below next to my name; THAT we verily believe we are the original, joint inventors of the invention entitled

A SERIAL-PARALLEL BINARY MULTIPLIER

the specification of which:

[ ] is attached hereto.
[X] was filed on June 1, 2001 as Application Serial No. 09/857,503 and was amended on _____ (if applicable).
[ ] is amended in the attached Amendment.

THAT we do not know and do not believe that this invention was ever known or used in the United States of America before our invention or discovery thereof, or patented or described in any printed publication in any country before our invention or discovery thereof, or more than one year prior to this application;

THAT the invention was not in public use or on sale in the United States of America for more than one year prior to this application;

THAT this invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months before this application;

THAT we have reviewed and understand the contents of the above identified specification, including the claim(s), as amended by any amendment referred to above;

THAT we acknowledge the duty to disclose information of which we are aware which is material to the examination of this application in accordance with 37 CFR §1.56; and

I HEREBY CLAIM foreign priority benefits under Title 35, United States Code §119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number	Country	Foreign Filing Date	Priority Claimed?	Certified Copy Attached?

Serial No. 09/857,503

I HEREBY CLAIM the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

U.S. Provisional Application Number	Filing Date

I HEREBY CLAIM the benefit under Title 35, United States Code, §120 of any United States application(s), or § 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application Number	PCT Parent Application Number	Parent Filing Date	Patent Parent Number
	PCT/GB99/03897	December 4, 1998	WO/00/34853

And I hereby appoint, as my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent; individually and collectively:

Foley & Lardner
2029 Century Park East, Suite 3500
Los Angeles, California 90067-3021

telephone number (310) 277-2223 (to whom all communications regarding the subject application are to be directed); and each attorney thereof named below with Registration Numbers, and of the same address:

Russell J. Barron	Reg. No. 29,612	Peter G. Mack	Reg. No. 29,001
Stephen A. Bent	Reg. No. 29,768	Brian J. McNamara	Reg. No. 32,789
David A. Blumenthal	Reg. No. 26,257	Sybil Meloy	Reg. No. 22,749
Edward W. Brown	Reg. No. 22,022	James G. Morrow	Reg. No. 32,505
John C. Cooper	Reg. No. 26,416	Ted R. Rittmaster	Reg. No. 32,933
Harry C. Engstrom	Reg. No. 26,876	Richard L. Schwaab	Reg. No. 25,479
William T. Ellis	Reg. No. 26,874	Bernhard D. Saxe	Reg. No. 28,665
John J. Feldhaus	Reg. No. 28,822		
Jack L. Lahr	Reg. No. 19,621		

and each attorney named below with Registration Number, of Advanced Micro Devices, Inc.; individually and collectively:

Elizabeth A. Apperley	Reg. No. 36,428	Richard J. Rodby	Reg. No. 27,588
Bradley Botsch	Reg. No. 34,852	Harry Wolin	Reg. No. 32,638
Michael Caywood	Reg. No. 37,757	Paul S. Drake	Reg. No. 33,491
Rajendra Jaipershad	Reg. No. 44,168	Daniel R. Collopy	Reg. No. 38,567

We declare further that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further

Serial No. 09/857,503

that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Inventor's Signature:
Date: WEDNESDAY 2nd JAN 2002
Inventor's Name (Typed): Andrew Dewhurst
First Middle Initial Family Name
Citizenship: British
Residence (City): 3 Bramble Close, Gentrys Green, Middlewich, Cheshire GBR
(State/Foreign Country): Great Britain
Post Office Address:

Inventor's Signature:
Date:
Inventor's Name (Typed):
First Middle Initial Family Name
Citizenship:
Residence (City):
(State/Foreign Country):
Post Office Address:
(Zip code)

Docket No. 078986-0203

DECLARATION AND POWER OF ATTORNEY

As below named inventors, we hereby declare: THAT my residence, post office address and citizenship is as stated below next to my name; THAT we verily believe we are the original, joint inventors of the invention entitled

A SERIAL-PARALLEL BINARY MULTIPLIER

the specification of which:

[ ] is attached hereto.
[X] was filed on June 1, 2001 as Application Serial No. 09/857,503 and was amended on _____ (if applicable).
[ ] is amended in the attached Amendment.

THAT we do not know and do not believe that this invention was ever known or used in the United States of America before our invention or discovery thereof, or patented or described in any printed publication in any country before our invention or discovery thereof, or more than one year prior to this application;

THAT the invention was not in public use or on sale in the United States of America for more than one year prior to this application;

THAT this invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months before this application;

THAT we have reviewed and understand the contents of the above identified specification, including the claim(s), as amended by any amendment referred to above;

THAT we acknowledge the duty to disclose information of which we are aware which is material to the examination of this application in accordance with 37 CFR §1.56; and

I HEREBY CLAIM foreign priority benefits under Title 35, United States Code §119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number	Country	Foreign Filing Date	Priority Claimed?	Certified Copy Attached?

Serial No. 09/857,503

I HEREBY CLAIM the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

U.S. Provisional Application Number	Filing Date

I HEREBY CLAIM the benefit under Title 35, United States Code, §120 of any United States application(s), or § 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application Number	PCT Parent Application Number	Parent Filing Date	Parent Patent Number
	PCT/GB99/03897	December 4, 1998	WO/00/34853

And I hereby appoint, as my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent; individually and collectively:

Foley & Lardner
2029 Century Park East, Suite 3500
Los Angeles, California 90067-3021

telephone number (310) 277-2223 (to whom all communications regarding the subject application are to be directed); and each attorney thereof named below with Registration Numbers, and of the same address:

Russell J. Barron	Reg. No. 29,512	Peter G. Mack	Reg. No. 26,001
Stephen A. Bent	Reg. No. 29,768	Brian J. McNamara	Reg. No. 32,789
David A. Blumenthal	Reg. No. 26,257	Sybil Meloy	Reg. No. 22,749
Edward W. Brown	Reg. No. 22,022	James G. Morrow	Reg. No. 32,505
John C. Cooper	Reg. No. 26,416	Ted R. Rittmaster	Reg. No. 32,933
Harry C. Engstrom	Reg. No. 26,876	Richard L. Schwaab	Reg. No. 25,479
William T. Ellis	Reg. No. 26,874	Bernhard D. Saxe	Reg. No. 28,665
John J. Feldhaus	Reg. No. 28,822		
Jack L. Lahr	Reg. No. 19,621		

and each attorney named below with Registration Number, of Advanced Micro Devices, Inc.; individually and collectively:

Elizabeth A. Apperley	Reg. No. 36,428	Richard J. Roddy	Reg. No. 27,688
Bradley Botsch	Reg. No. 34,552	Harry Wolin	Reg. No. 32,638
Michael Caywood	Reg. No. 37,797	Paul S. Drake	Reg. No. 33,491
Rajendra Jaipershad	Reg. No. 44,168	Daniel R. Collopy	Reg. No. 33,667

We declare further that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further

Serial No. 09/857,503

that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Inventor's Signature: _____

Date: Monday 6th August 2001

Inventor's Name (Typed): Andrew Dewhurst

First **Middle Initial** **Family Name**

Citizenship: GBR

Residence (City): 3 Bramble Close, Gentrys Green, Middlewich, Cheshire

(State/Foreign Country): Great Britain

Post Office Address: _____

_____

Inventor's Signature: _____

Date: _____

Inventor's Name (Typed): _____

First **Middle Initial** **Family Name**

Citizenship: _____

Residence (City): _____

(State/Foreign Country): _____

Post Office Address: _____

_____ (Zip code)